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INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.

(RIGHT OUTSIDE)

DOCUMENT-IDENTIFIER: US 6258665 B1
TITLE: Non-volatile semiconductor memory device and method for manufacturing the same

DEPR:

Next, as shown in FIG. 26, an insulating material such as TEOS or BPSG is deposited over the whole surface, whereby the openings and the trenches 111 formed in the laminated structure consisting of the tunnel oxide film 105, the polycrystalline silicon film 106 and the nitride film 201 are filled up with a filling or burying material 112. Then, the surface of the thus deposited burying material 112 is flattened. This flattening operation is carried out by the use of, e.g. the etch-back method using anisotropic etching or the like.

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Shimizu et al.

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(13) Date of Patent: Jul. 10, 2001

(14) NON-VOLATILE SEMICONDUCTOR
MEMORY DEVICE AND METHOD FOR
MANUFACTURING THE SAME

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Kazuo Nakano, et al. (JP)

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(18) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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(20) ABSTRACT

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Related U.S. Application Data

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1998, now Pat. No. 5,583,971.

(24) Foreign Application Priority Data

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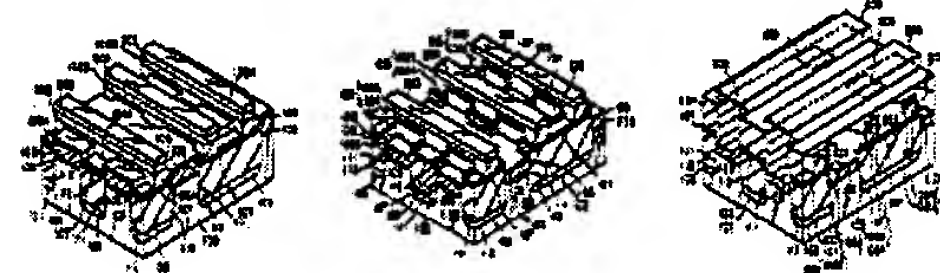
(25) Int. Cl. H01L 21/0247

(26) U.S. Cl. 438/257; 437/51

(27) Field of Search 438/257, 437/51,
436/211, 553, 559, 563, 567, 569, 570, 571, 572

The non-volatile semiconductor memory device is formed on a silicon substrate and comprises a plurality of semiconductor active regions defined by a plurality of element isolation regions, a source region and a drain region formed in each of the semiconductor active regions, a charge storage layer which capacitively couples to the semiconductor active region between the source region and the drain region, and a control gate which capacitively couples to the charge storage layer through a tunnel gate insulating film, wherein the tunnel gate insulating film is left extending from the upper surface portion of the element isolation region which lies under the control gate to the upper surface portion of the element isolation region other than the upper surface portion of the element isolation region lying under the control gate.

8 Claims, 26 Drawing Sheets



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